#### GATE MODULATION FOR HIGH POWER AMPLIFIERS

#### REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on July 16, 2003, and the references cited therewith.

No claims were amended or added. Claims 1, 5-7, and 15-21 are now pending in this application.

## \$102 Rejection of the Claims

Claims 1 and 21 were rejected under 35 USC § 102(b) as being anticipated by Kusunoki (U.S. 5,471,656). This rejection is respectfully traversed.

The Office action equates the power supply to a bias signal in Figure 1 of Kusunoki. Kusunoki recites the problems of switching the power supply on and off to the power amplifier 4: "The first defect is that the power source voltage of the power amplifier 4 is intermittently on and off. In this case, since many capacitors are inserted in the power source terminal of the power amplifier 4, it is impossible to turn on and off the power source voltage at a high speed..." Col. 1, lines 61-65. Further, "average efficiency of the terminal device is degraded" as indicated in Col. 2, lines 11-12.

Thus, the statement in the Office Action: "...Kusunoki discloses a method of controlling an RF power amplifier 4 wherein during the low points in the input signal, the bias, i.e. power supply is removed so as to reduce power consumption." is incorrect. First, the power supply is not a bias signal. Kusunoki makes this clear with respect to the description of FIG. 2, the gate bias generator 13. The gate bias generator is low when the high frequency signal is small, and is high when the high-frequency signal is large. Thus, it is clearly not a power supply, since the voltage seems to vary significantly, and the plain meaning of a bias signal makes it clear it is not a power supply. Second, Kusunoki clearly states that such an arrangement as shown in FIG. 1 degrades the efficiency of the terminal device.

The Office Action refers to the power source 3 of Kusunoki as providing a bias signal. This is also traversed. It is clearly a power supply, and not a bias signal. Kusunoki clearly states that the power source voltage of the power amplifier 4 is intermittently on and off, not that a bias signal is removed when the magnitude of the input signal reaches a predetermined threshold.

RESPONSE UNDER 37 CFR § 1.116 - EXPEDITED PROCEDURE

Serial Number: 09/888823

Filing Date: June 25, 2001

Title: GATE MODULATION FOR HIGH POWER AMPLIFIERS

Page 7 Dkt: 778.042US1

Kusunoki goes on to indicate that the bias signal applied to the amplifier 11 is low or high, not that it is removed as claimed in claims 1 and 21.

Claim 21 further recites that the bias signal is relatively static when the magnitude of the input signal falls below a predetermined threshold. The bias signal in Kusunoki as seen in FIG. 2 is the sum of the control signal and the gate bias generator 13 signal as added in adder 15 and presented at gate bias terminal 17 in amplifier 11. There is no indication that the bias signal provided to the gate bias terminal 17 is relatively static as claimed.

Since claims 3, 4, and 8 depend from claim 1, they are also allowable without further search required. Therefore, it is requested that such claims be reinstated.

## §103 Rejection of the Claims

Claims 5-7 were rejected under 35 USC § 103(a) as being unpatentable over Kusunoki in view of Pan et al. (U.S. 5,920,596). This rejection is respectfully traversed at least on the basis that claim 1 is believed allowable over Kusunoki.

Claim 20 was rejected under 35 USC § 103(a) as being unpatentable over Faulkner et al. (U.S. 5,420,536) in view of Kusunoki. This rejection is respectfully traversed. Claim 20 recites that the bias signal is in and on or off state. As indicated above, Kusunoki provides a bias signal that is never in an off state. Faulkner et al. also does not show or suggest such a bias signal.

Claims 15-19 are allowed.

Page 8 Dkt: 778.042US1

Serial Number: 09/888823 Filing/Date: June 25, 2001

GATE MODULATION FOR HIGH POWER AMPLIFIERS

# **CONCLUSION**

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 373-6972 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

TREVOR A. PAGE

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. P.O. Box 2938

Minneapolis, MN 55402

(612) 373-6972

Date 9-11-2003

Bradley X. Forrest

Reg. No. 30,837

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this \_\_\_\_\_\_ day of September, 2003.

Candis B. Buending

Name

Signature

SEP 29 2003